IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Mark D. Matson; Bruce E. Edwards		
Assignee:	Broadcom Corporation		
Title:	MAC Controlled Sleep Mode/Wake-up Mode with Staged Wake-up for Power Management Devices		
Serial No.:	10/810,094	Filed:	March 26, 2004
Examiner:	Andrew Wendell	Group Art Unit:	2618
Docket No.:	BP 3197	Customer No.:	34399

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Austin, Texas
October 9, 2007

PRE-APPEAL BRIEF REQUEST FOR REVIEW AND STATEMENT OF REASONS

Sir:

Applicants request review of the Final Office Action in this application. No amendments are being filed with the request. This request is being filed with a Notice of Appeal. The following sets forth a succinct, concise, and focused set of arguments for which the review is being requested.

CLAIM STATUS

In the final Office Action, the Examiner rejected claims 11-18 under 35 U.S.C. § 101, but indicated that the rejection could be overcome by including a "computer readable medium encoded with a computer program" limitation in the claims. In addition, claims 1, 2, 4-6, 8, 10-11, 13-14 and 16-18 were rejected as anticipated by U.S. Patent No. 6,473,607 to Shohara et al.; claim 3 was rejected as obvious over Shohara in view of U.S. Patent Publication No. 2003/0028677 to Fukuhara; claims 7, 12 and 19-20 were rejected as obvious over Shohara in view of U.S. Patent No. 6,622,251 to Lindskog et al.; and claims 9 and 15 were rejected as obvious over Shohara in view of U.S. Patent Publication No. 2002/0059434 to Karaoguz et al. Applicant's after final attempt to amend claims 19-20 to clarify the "instruction pipeline" requirement was denied in the September 21, 2007 Advisory Action. As explained below, Applicants traverse these rejections because (1) the Applicants' amendment to claims 11-18 to overcome the rejection under 35 U.S.C. § 101 as suggested by the Examiner was improperly denied, and (2) none of the cited art references meet the "instruction pipeline" limitation variously recited in the claims.

A. Amended Claims 11-18 Recited Statutory Subject Matter

In response to the Examiner's final rejection of claims 11-18 under 35 U.S.C. § 101, Applicants amended the claims as suggested by the Examiner. Because this amendment was

submitted to comply with a requirement of form set forth in the previous Office Action, Applicants submit that the amendment was permitted under 35 CFR § 1.116(b)(1), and therefore respectfully request that the statutory subject matter rejection of claims 11-18 under 35 U.S.C. § 101 be withdrawn and that the amended claims be allowed.

B. Claims 1, 2, 4-6, 8, 10, 11, 13-14 and 16-18 Are Not Anticipated by Shohara

In response to the Examiner's previous rejection of claims 1, 2, 4-6, 8, 10, 11, 13-14 and 16-18 under 35 U.S.C. § 102 as being anticipated by Shohara, Applicants explained that Shohara fails to disclose an "instruction pipeline circuit," much less Applicants' scheme for using detected sleep instructions and wakeup signals to selectively power down and reactivate processing modules in the instruction pipeline circuit only to the extent required by the sleep instruction and the wake-up signal. To underscore this deficiency, Applicants pointed out that the word "pipeline" never appears in Shohara, a fact that was not disputed by the Examiner. In the Final Office Action, the Examiner responds to this deficiency by proposing an unreasonably broad and wholly unsupported definition of "instruction pipeline" and then asserting that Shohara meets this overbroad definition. In particular, the Examiner asserts that "any circuit that carries out instructions (i.e. control information) to other components through channels (i.e. connections) can be considered an instruction pipeline given the broadest responsible (sic, reasonable) interpretation." Final Office Action, p. 9 (June 6, 2007). With all due respect, this is simply not a reasonable interpretation of the "instruction pipeline" term. As explained more fully below, when the *proper* interpretation of the "instruction pipeline" term is used, Shohara simply does not meet the requirements of the claims.

1. Correct Interpretation of "Instruction Pipeline"

According to the MPEP Guidelines, the pending claims must be "given their broadest reasonable interpretation consistent with the specification" during patent examination. *See*, MPEP § 2111. This was confirmed with the Federal Circuit statement that:

> The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

Phillips v. AWH Corp., 415 F.3d 1303, 1316, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005). Thus, "the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468

(Fed. Cir. 1999). "This means that the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification." *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). "The ordinary and customary meaning of a term may be evidenced by a variety of sources, including 'the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.'" MPEP § 2111.01, *citing Phillips v. AWH Corp.*, 415 F.3d at 1314, 75 USPQ2d at 1327.

Based on the foregoing, Applicants submit that the "instruction pipeline" refers to a processing structure that separates the execution of instructions into multiple stages (e.g., instruction fetch, instruction decode and operand read, execution, and write), and executes separate instructions in each stage simultaneously, thereby allowing multiple instructions to be executed concurrently. As depicted in the application, each stage simultaneously processes its assigned set of signals, and then forwards the results of the processing to the next stage and receives from the prior stage the results of the prior stage's processing. The resulting overlap of operations by each stage increases the overall throughput of the processor structure. Applicants' proposed interpretation is consistent with the specification as it would be interpreted by one of ordinary skill in the art. *See, e.g.*, Application, Figure 3 ("instruction pipeline circuit 140") and paragraphs 30, 32, 33, 35-38 and 41. *See*, MPEP § 2111, *citing In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). In addition, Applicants' proposed interpretation is consistent with the "ordinary and customary meaning" as evidenced by substantial extrinsic evidence previously submitted, including Wikipedia's definition of "Instruction Pipeline"; J. Silc et al., Processor Architecture, pp. 18-20, 349 and 354 (1999) ("instruction pipeline"); D. Patterson et al., Computer Architecture: A Quantitative Approach, pp. 251-252 (1990) ("pipelining"); W. Rosch, The Winn L. Rosch Hardware Bible, Third Edition, pp. 44-45 (1994) ("pipelining"); Microsoft Computer Dictionary p. 367 (3rd ed. 1997) ("pipelining"); and H. Messmer, The Indispensable PC Hardware Book, pp. 216-218, 1239 and 1250-1251 (4th ed. 2002) ("instruction pipelining"). If there is any reputable extrinsic evidence that supports the Examiner's proposed interpretation here, Applicants would request that it be provided. However, based on Applicants' review, Applicants' proposed interpretation is consistent with the specification and with the submitted extrinsic evidence definitions which better reflect how one of ordinary skill in the art would interpret the "instruction pipeline" term.

2. Shohara Does Not Meet The Properly Interpreted "Instruction Pipeline" Requirement

As explained above, the broadest reasonable interpretation of the "instruction pipeline" term that is consistent with the specification (and confirmed by the extrinsic evidence) refers to a

processing structure that separates the execution of instructions into multiple stages (e.g., instruction fetch, instruction decode and operand read, execution, and write), and executes separate instructions in each stage simultaneously, thereby allowing multiple instructions to be executed concurrently. This requirement is simply not met by Shohara's disclosure of using an "event scheduler" to control reception of "scheduled intermittent messages" with a dual mode timer that uses different clock signals to power down all idle components during a scheduled power save sleep mode. Accordingly, Shohara does not anticipate the present invention's claimed scheme detecting a "sleep instruction" which is used to place the processing unit, instruction pipeline circuit and at least one processing module in a low-power state, and then reactivating the instruction pipeline circuit to the extent required by a received "wake-up signal." *See, e.g.*, claims 1 and 11. Accordingly, Applicants respectfully request that the anticipation rejection of claims 1, 2, 4-6, 8, 10, 11, and 13-14 and 16-18 be withdrawn and that the claims be allowed.

C. Claims 3, 7, 9, 12, 15 and 19-20 Are Not Obvious

In response to the Examiner's obviousness rejections of claims 3, 7, 9, 12, 15 and 19-20, Applicants submit that a *prima facie* case of obviousness has not been established showing that all the claim limitations are taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). First of all, claims 3, 7, 9, 12, 15 and 20 each include an "instruction pipeline" requirement (either expressly or by virtue of their dependency from claims 1 and 11)[1]. As explained above, the broadest reasonable interpretation of the "instruction pipeline" term that is consistent with the specification (and confirmed by the extrinsic evidence) refers to a processing structure that separates the execution of instructions into multiple stages (e.g., instruction fetch, instruction decode and operand read, execution, and write), and executes separate instructions in each stage simultaneously, thereby allowing multiple instructions to be executed concurrently. This requirement is simply not met by Shohara's disclosure, either alone or in combination with the other cited references, of using an "event scheduler" to control reception of "scheduled intermittent messages" with a dual mode timer that uses different clock signals to power down all idle components during a scheduled power save sleep mode.

In addition, Applicants submit that the cited references do not disclose or suggest Applicants' claimed invention for controlling power in a communications processor by responding to "sleep instructions" and "wake-up signals" to selectively reactivate only the processor modules in the instruction pipeline circuit that are required to respond to the detected

[1] While the Examiner denied Applicants' after final amendments to claims 19-20 (adding the "instruction pipeline circuit" limitation), Applicants submit that the "instruction pipeline circuit" limitation was

wake-up signal. Shohara's failure to disclose an "instruction pipeline circuit" is not remedied by the Fukuhara, Lindskog or Karaoguz references, none of which refer to a "pipeline circuit." Nor do the cited references, alone or in combination, disclose or suggest a communication processor which goes to sleep at arbitrary times (via the sleep instruction) and which can be awakened by external events (via wake-up signals) which can occur at any time. Nor do the cited references disclose that the individual modules in the instruction pipeline circuit can be reactivated only to the extent required by the wake-up instruction. Indeed, the Shohara disclosure seems to directly contradict the idea of selective power-up. *See*, Shohara Patent, col. 12, lines 32-56. On this point, Shohara is quite clear that the Shohara controller "powers down all idle components of the device between message receptions in a power saving sleep mode to conserve battery power. During active mode when the device is fully active in reception of messages the timer uses a reference oscillator with a relatively high frequency to support digital processing by the receiver." Shohara Patent, col. 10, lines 39-44. When, as here, the Shohara reference teaches away from the claimed invention, a *prima facie* case of obviousness has been rebutted. *See*, MPEP § 2144.05(III) ("A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. In re Geisler, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997)…."). Based on the foregoing, Applicants request that the obviousness rejection of claims 3, 7, 9, 12, 15 and 19-20 be withdrawn and that the claims be allowed.

CONCLUSION

In view of the remarks and amendments set forth herein, Applicants respectfully submit that all pending claims are in condition for allowance and request that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

/Michael Rocco Cannatti/

Michael Rocco Cannatti
Attorney for Applicants
Reg. No. 34,791

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included in the original claim 20. If it is determined that this limitation is not disclosed in the prior art, Applicants reserve the right to amend claim 19 to incorporate the limitations of claim 20.